REMARKS

Claims 1 and 3-18 are pending in the application. Claims 1, 7 and 13 have been amended, and no claims have been added or canceled by this response. Thus upon entry of this paper, claims 1 and 3-18 will continue to be pending in the application. Support for the claim amendments can be found in paragraphs **[0025]** through **[0031]** of the specification.

In the outstanding Office Action, claims 1, 3-6, 13-16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicants prior art figure 2B (APAF) in view of U.S. Patent Publication 20020122280 (Ker et al) and U.S. Patent 6,194,776 (Amano); claims 7, 8, 10-12, and 17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over the APAF in view of Ker et al. Reconsideration is respectfully requested.

35 U.S.C. 103 Rejections

In the outstanding Office Action, claims 1, 3-6, 13-16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art (APA) in view of Ker et al. and Amano. Moreover, claims 7, 8, 10-12 and 17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over the APAF in view of Ker et al. Applicants respectfully disagree with these conclusions and traverse this rejection as follows.

The APA referred to in the outstanding Office Action discloses a conventional implementation of an ESD NMOSFET. Ker et al. discloses an ESD protection component with a deep-N-well structure. The ESD protection component comprises a lateral silicon controlled rectifier (SCR) and a deep N-well. The SCR comprises a P-type layer, an N-type layer, a first N-well and a first P-well. The P-type layer is used as an anode of the SCR; the N-type layer is used as a cathode of the SCR; the first N-well is located between the P-type layer and the N-type layer and is contacted with the P-type layer; and the first P-well is contacted to the first N-well and the N-type layer. The deep N-well is located between the first P-well and the P-substrate, and is used to isolate the electric connection between the P-substrate and the first P-well. A plurality of these

ESD protection components arbitrarily connected in series increases the total holding voltage of ESD protection circuit, thus preventing occurrences of latch-up.[1]

Amano discloses a semiconductor circuit device having a triple-well structure wherein a predetermined potential level is supplied to a top well without a contact region formed in the top well is disclosed. In an N-type ion implantation step for forming an N-type well region (1) in a P-type semiconductor substrate (5), a mask of a predetermined configuration is used so that ions are not implanted into a region of a portion which is to serve as a bottom portion (1B) of the well region (1). Then, the N-type well region (1) is formed which is shaped such that a portion (6) having P-type properties remains partially in the bottom portion (1B). The P-type portion (6) establishes electrical connection between a P-type well region (2) and the semiconductor substrate (5) to permit the potential applied to a contact region (4) to be supplied to the well region (2) therethrough. The portion (6) may include a plurality of portions (6) which allow uniform potential supply. This structure may be applied to basic cells of a memory cell array block.[2]

Ker et al. fails to disclose, as amended claim 1 recites in pertinent part:

> [A] source and drain region in said first well forming an FET, said drain being connected to an I/O pad for protecting said pad against an ESD event; and
>
> *a path of substrate material extending through a single opening in said segmented conductive band to increase substrate resistance by creating a single extended path for current which flows through said I/O pad to substrate contacts and drain during an ESD event and electrically connecting the first well to the substrate*,
>
> wherein the second and third wells are completely isolated from the drain, source and substrate contacts by shallow trench isolation structures, and
>
> wherein the substrate contacts are located outside the first, second and third wells and directly connected to the substrate (emphasis added).

[1] See Ker et al. at Abstract.
[2] See Amano at Abstract.

That is, in the present invention, the path that extends through the single opening increases substrate resistance by *creating a single extended path for current which flows through said I/O pad to substrate contacts and drain during an ESD event.* In this regard, the single opening recited in claim 1 plays an the role of limiting the current flow to the single extended path. That is, by providing a single opening through which current flows, a single, extended, current pathway through the opening is established yielding consistent and potentially larger substrate resistance then would be provided by a similar structure with *a plurality of openings that provide multiple current pathways*. In contrast to the claimed invention, Ker et al., as indicated in the outstanding Office Action, discloses a plurality of openings is provided in the conductive band region. Intuitively, such a plurality of openings would serve to reduce the substrate resistance (i.e., due to the multiple current pathways which is similar to resistances in parallel which are always lower in resistance than one in series) and *not* increase the resistance by providing a range of current pathways of differing lengths. The different pathway lengths would correspond to different substrate resistance values with an overall substrate resistance value tending to a lower value (i.e., the above-discussed parallel resistance concept) rather than the increased substrate resistance generated by the "single extended pathway," as recited in amended claim 1of the present invention. Thus, contrary to the assertions made in the outstanding Office Action, the single opening feature recited in claim 1 is patentably distinguishing. Moreover, neither Amano nor the APA can make up for this deficiency in Ker et al.

Claim 13 reciting language similar to that in amended claim 1 recites in pertinent part:

> [A] resistive path extending through a *single* opening in said segmented conductive band region to said substrate contacts, said resistive path *minimizing* the trigger voltage for said FET (emphasis added).

That is, in the present invention, a current pathway through a single opening lends itself to minimizing the trigger voltage of an FET in accordance with the present invention. Applicant respectfully submits, therefore, that none of the APAF, Ker et al. and Amano whether taken alone or in combination, disclose the present invention and that claims 1 and 13 patentably

distinguish thereover. Applicant, therefore, respectfully requests that the rejections of claims 1 and 13 under 35 U.S.C. 103 (a) be withdrawn. Moreover, claims 3-6, and 14-16 and 18 are respectively dependent on independent claims 1 and 13. Accordingly claims 3-6, 14-16 and 18 are patentable for at least the same reasons that independent claims 1 and 13 are patentable.

With respect to the rejection of claims 7, 8, 9, 10-12, and 17, Applicant responds as follows.

Amended claim 7 recites in pertinent part:

> providing a resistive path extending through a single opening in a segmented conductive band from said well to substrate contacts located outside of said wells, whereby the trigger voltage of the said ESD NMOSFET is *minimized* due to *the length of* said resistive path between said substrate contacts and said I/O pad (emphasis added).

As discussed above in conjunction with the rejections of claim 1 and 13, the length of the resistive path in the present invention minimizes the trigger voltage of a device in accordance with the present invention. Applicant therefore respectfully submits that neither the APAF nor Ker et al., whether taken alone or in combination, discloses the present invention and that claim 7 patentably distinguishes thereover. Applicant, therefore, respectfully requests that the rejections of claim 7 under 35 U.S.C. 103 (a) be withdrawn. Moreover, claims 8, 9, 10-12 and 17 are dependent on independent claim 7. Accordingly, claims 8, 9, 10-12 and 17 are patentable for at least the same reasons that independent claim 7 is patentable.

CONCLUSION

Applicant believes no fee is due with this response. However, the Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our

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